Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1–7 (canceled)

Claim 8 (currently amended). ~~An ingress/egress port for an Ethernet switch.~~ An Ethernet switch including a plurality of ports (n), each port comprising:

an ingress/egress port;

a plurality of Media Access Control (MAC) interfaces, each MAC interface is capable of receiving/transmitting Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configurable to receive/transmit Gigabit Ethernet (GE) packets; ~~and~~

receive and transmit modules which are configurable respectively to receive both GE and FE packets from, and transmit GE and FE packets to, the interfaces; and

wherein at least a portion of the plurality of ports are switchable between two modes in which the portion of the plurality of ports operate respectively as one GE port or a plurality of FE ports (m), and wherein there are m MAC interfaces per port, wherein the switch is configured to operate as n GE ports and m (m-n) FE ports where n is a selectable integer greater than 1 and m is an integer greater than 1.

Claim 9 (currently amended). The ~~port~~ switch according to claim 8 wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets, the other MAC interfaces only being adapted to receive/transmit FE packets.

Claim 10 (currently amended). The ~~port~~ switch according to claim 9 wherein which each MAC interface is associated with a buffer configured to store packets as they are received, the receive module being arranged to receive packets from the buffers sequentially, whereby the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

Claim 11 (currently amended). The ~~port~~ switch according to claim 8 wherein which each MAC interface is associated with a buffer configured to store packets as they are received, the receive module being arranged to receive packets from the buffers sequentially, whereby the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

Claim 12 (currently amended). The ~~port~~ switch according to claim 8 wherein the receive module further includes a memory configured to store packet data, and a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

Claim 13 (currently amended). The ~~port~~ switch according to claim 12, wherein the receive module further comprises a set of buffers configured to receive packets from at

least one of the MAC interfaces, and wherein the receiver interface is further operable to fetch packet data from the set of buffers and store the packet data in the memory.

Claim 14 (currently amended). The ~~port~~ switch according to claim 13, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

Claim 15 (currently amended). The ~~port~~ switch according to claim 13, wherein the receiver interface is further operable to store the descriptor associated with the packet data in the memory.

Claim 16 (currently amended). A ~~port~~ switch according to claim 8 wherein the plurality of MAC interfaces consists of 8 MAC interfaces.

Claim 17 (currently amended). An Ethernet switch comprising:

a plurality of ports (n), each port including

an ingress/egress port, ~~for an Ethernet switch having~~

a plurality of Media Access Control (MAC) interfaces, each MAC interface ~~is~~ capable of receiving/transmitting Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configurable to receive/transmit Gigabit Ethernet (GE) packets, ~~and~~

receive and transmit modules which are configurable respectively to receive both GE and FE packets from, and transmit GE and FE packets to, the interfaces; and

wherein at least a portion of the plurality of ports are switchable between a first mode and a second mode, wherein the portion of the plurality of ports operate as a single GE port in the first mode and the portion of the plurality of ports operate as multiple FE ports (m) in the second mode, wherein there are m MAC interfaces per port, and wherein the Ethernet switch can operate as n GE ports and m (m-n) FE ports where n is a selectable integer greater than 1 and m is an integer greater than 1

~~at least one other ingress/egress port~~.

Claim 18 (cancelled).

Claim 19 (currently amended). The Ethernet switch according to claim ~~18~~ 17, wherein the plurality of ports comprise ~~ingress/egress port and the other ingress/egress ports total~~ eight ingress/egress ports, ~~each ingress/egress port being switchable between two modes, a first mode operating as one GE port and a second mode operating as eight FE ports,~~ and wherein the switch can operate as *n* GE ports and 8(8-*n*) FE ports.

Claim 20 (previously presented). The Ethernet switch according to claim 17, wherein the receive module further includes a memory configured to store packet data, and a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

Claim 21 (previously presented). The Ethernet switch according to claim 20, wherein the receive module further comprises a set of buffers configured to receive packets from at

least one of the MAC interfaces, and wherein the receiver interface is further operable to fetch packet data from the set of buffers and store the packet data in the memory.

Claim 22 (previously presented). The Ethernet switch according to claim 21, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

Claim 23 (previously presented). The Ethernet switch according to claim 21, wherein the receiver interface is further operable to store the descriptor associated with the packet data in the memory.

Claim 24 (currently amended). A method, comprising

providing data packets to an ingress/egress port of an Ethernet switch having a plurality of ports (n), each of the plurality of ports having an~~, the~~ ingress/egress port and having a plurality of Media Access Control (MAC) interfaces, each of ~~which is~~ the plurality of MAC interfaces capable of receiving/transmitting Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configurable to receive/transmit Gigabit Ethernet (GE) packets; and

passing packet data from the data packets ~~from the ingress/egress ports~~ to one or more receive modules, the one or more receive modules configurable to receive both GE and FE packets; ~~and~~

passing outgoing packet data from one or more transmit modules to the ~~ingress/egress port~~ interfaces, the one or more transmit modules configurable to transmit both GE and FE packets; and

switching at least a portion of the plurality of ports between two modes, wherein the portion of the plurality of ports operate as one GE port in a first mode and a plurality of FE ports (m) in a second mode, wherein there are m MAC interfaces per port, and wherein the switch is configured to operate as n GE ports and m (m-n) FE ports where n is a selectable integer greater than 1 and m is an integer greater than 1.

Claim 25 (currently amended). The method according to claim 24, further comprising providing a control signal ~~to the ingress/output port~~ to determine whether the MAC interfaces operate as FE interfaces or whether the at least one interface operates as a GE interface.

Claim 26 (previously presented). The method according to claim 25, wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets, and the other MAC interfaces are only adapted to receive/transmit FE packets.

Claim 27 (previously presented). The method according to claim 24, wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets, and the other MAC interfaces are only adapted to receive/transmit FE packets.